Applying Models of Computation to OpenCL Pipes for FPGA Computing

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Outline

- Models of Computation and Parallelism
    - OpenCL code samples
- Synchronous Dataflow (SDF)
- Bulk Synchronous Parallel (BSP)

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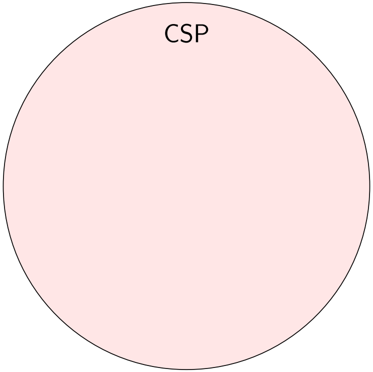
- In this proposal, OpenCL compute model + MoC Communication Schemes

Models of Computation Taxonomy



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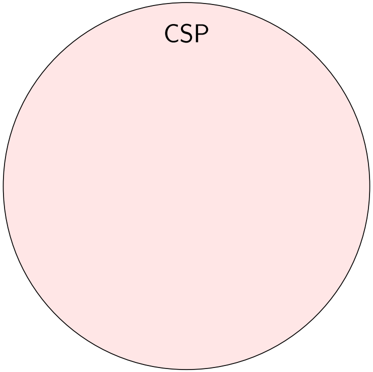

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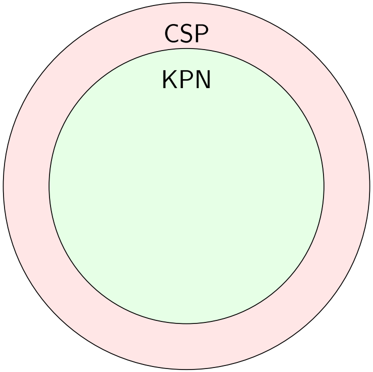

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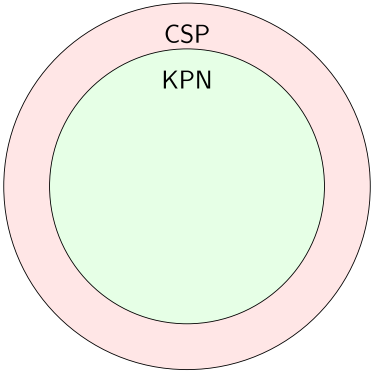

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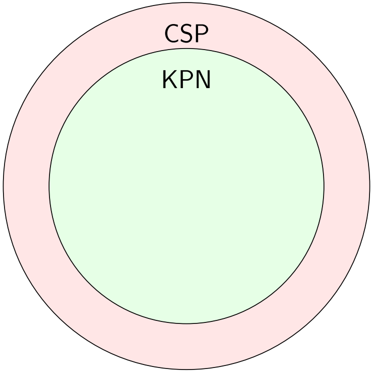

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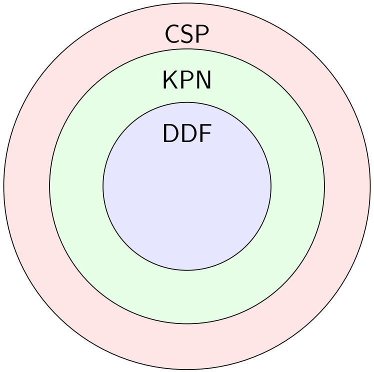

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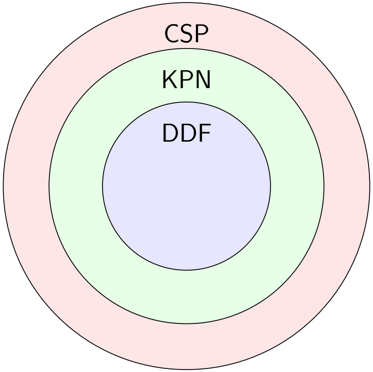

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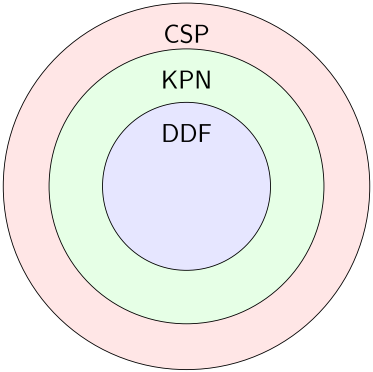

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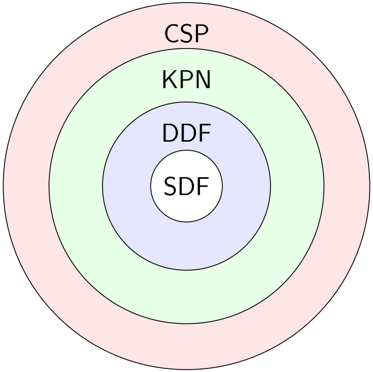

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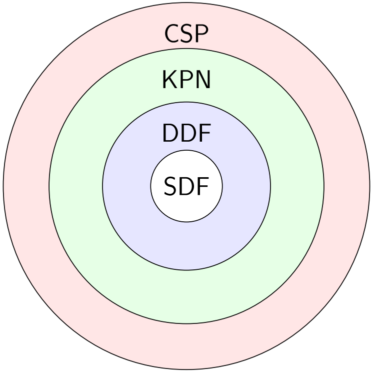

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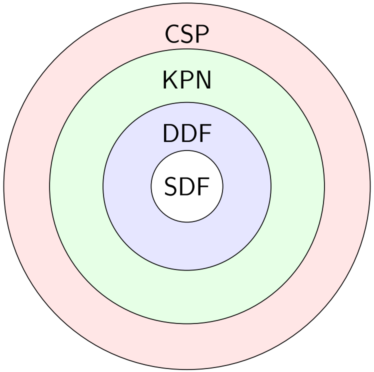

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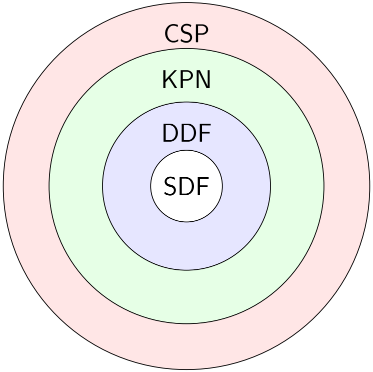

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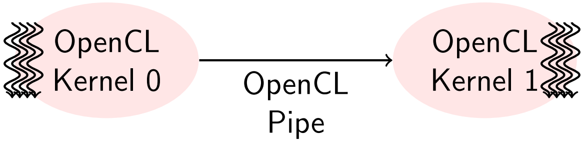
- `http://ptolemy.eecs.berkeley.edu`

Quick Intro to OpenCL Pipes

- Pipes provide a **disciplined** way to share data between kernels + allow overlapped multi-kernel operation
- Buffering of data between the producer-consumer pair possible



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- On-chip BRAMs can be configured as FIFOs

OpenCL code sketches (CSP)

```
//  aoc --board de5a_net_i2 csp.cl -o csp.aoco -c --report

__kernel void csp_kernel0(__global int* x, __write_only pipe int c0)
{
 int i=get_local_id(0);
 int done=-1, temp=0;
 temp = x[i]*x[i]; // dummy compute
 while(done!=0) {
  done = write_pipe(c0, &temp);
 }
}

__kernel void csp_kernel1(__global int* y, __read_only pipe int c0)
{
 int i=get_local_id(0);
 int done=-1, temp=0;
 while(done!=0) {
  done=read_pipe(c0,&temp);
 }
 y[i]=temp;
}
```

OpenCL code sketches (KPN)

```
//  aoc --board de5a_net_i2 kpn.cl -o kpn.aoco -c --report
#define INF 16

__kernel void kpn_kernel0(__global int* x,
  __write_only pipe int __attribute__((depth(INF))) c0)
{
 int i=get_local_id(0);
 int done=-1, temp=0;
 temp = x[i]*x[i]; // dummy compute
 done = write_pipe(c0, &temp);
 if(done!=0){printf("Unbounded FIFO cannot be full");}
}

__kernel void kpn_kernel1(__global int* y,
  __read_only pipe int __attribute__((depth(INF))) c0)
{
 int i=get_local_id(0);
 int done=-1, temp=0;
 while(done!=0) {
  // cannot read empty pipe
  done=read_pipe(c0,&temp);
 }
 y[i]=temp;
}
```

OpenCL code sketches (DDF)

```
//  aoc --board de5a_net_i2 ddf.cl -o ddf.aoco -c --report
#define INF 16
int get_pipe_num_packets(__read_only pipe int x) {return 0;}
__kernel void ddf_kernel0(__global int* x,
  __write_only pipe int __attribute__((depth(INF))) c0)
{
 int i=get_local_id(0);
 int done=-1, temp=0;
 while(done!=0) {
  temp = x[i]*x[i]; // dummy compute
  done = write_pipe(c0, &temp); // done=0 is guaranteed
 }
}
__kernel void ddf_kernel1(__global int* y,
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{
 int i=get_local_id(0);
 int done=-1, temp=0;
 while(done!=0 && get_pipe_num_packets(c0)>0) {
  done = read_pipe(c0,&temp); // done=0 is guaranteed
 }
 y[i]=temp;
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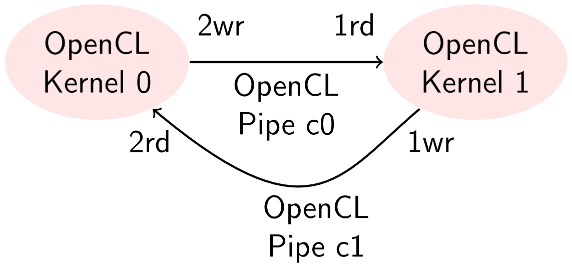
- Feedback loops or cycles not supported? Initial value problem.

SDF Model for OpenCL Pipes

- Synchronous Dataflow model ideal for **streaming** computation



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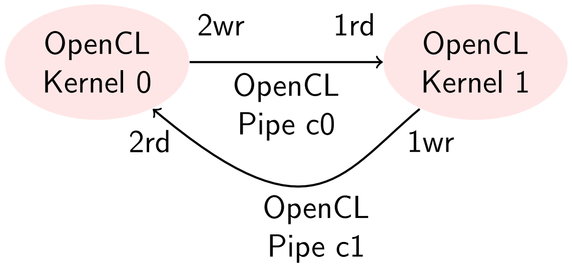

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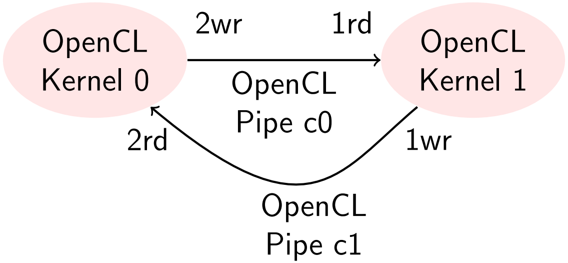

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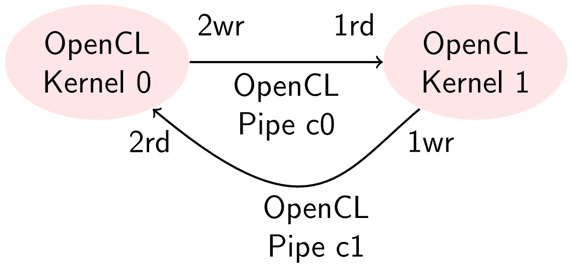

```
__kernel void sdf_kernel0(__read_only pipe int __attribute__((sdf)) c1,
  __write_only pipe int __attribute__((sdf)) c0)
{
 int i=get_local_id(0);
 int temp1=0, temp2=0, result1=0, result2=0;
 // no need to check FIFO full/empty
 read_pipe(c1, &temp1);
 read_pipe(c1, &temp2);
 result1 = temp1*temp2; // dummy compute
 result2 = temp2/temp1; // dummy compute
 write_pipe(c0, &result1);
 write_pipe(c0, &result2);
}

__kernel void sdf_kernel1(__write_only pipe int __attribute__((sdf)) c1,
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{
 int i=get_local_id(0);
 int temp=0, result=0;
 // no need to check FIFO full/empty
 read_pipe(c0,&temp);
 result=temp/10; // dummy compute
 write_pipe(c1,&result);
}
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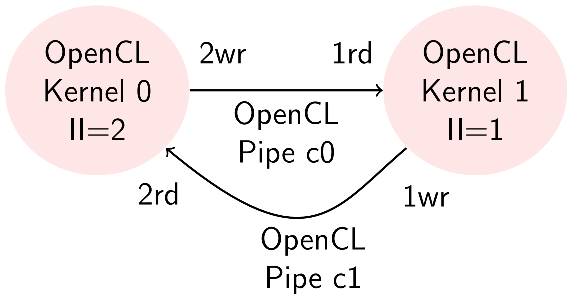
        - Consider FIFO port bandwidth constraint during HLS scheduling

Example FPGA Mapping Options

- *e.g.* Firing sequence: Kernel 0, Kernel 1, Kernel 1



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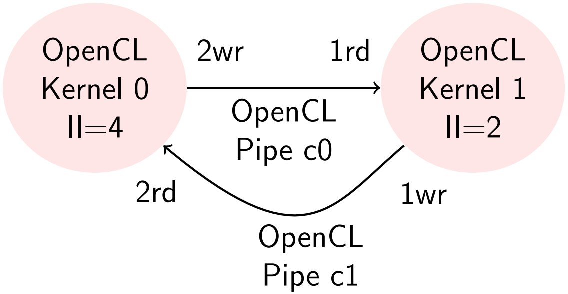
- *e.g.* Firing sequence: Kernel 0, Kernel 1, Kernel 1
- *e.g.* Kernel 0 II: x, Kernel 1 II: $\frac{x}{2} \rightarrow$ can save area by using higher II constraint on kernel 0



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- SDF allows multiple reads/write from same work-item
- Compiler determines depth attribute on pipes + area allocated to each kernel (subject to II minimization)

BSP Model for OpenCL Pipes

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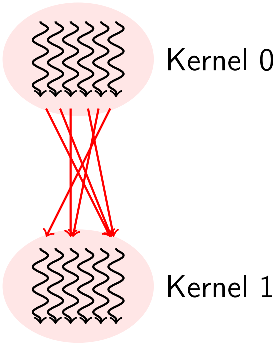

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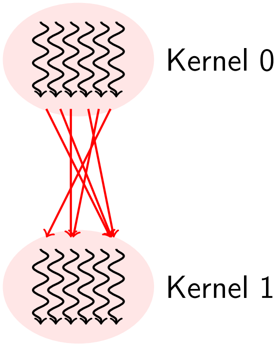

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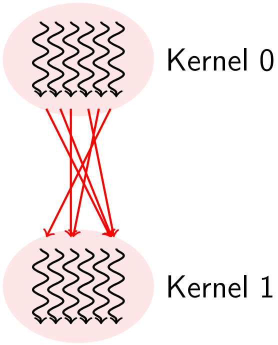

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__kernel void bsp_kernel0(__global int* x,
  __global int* dest,
  __write_only pipe int __attribute__((bsp)) c)
{
 int i=get_local_id(0);
 write_bsp_pipe(c, x[i], dest[i]);

 barrier(CLK_BSP_MEM_FENCE);
}

__kernel void bsp_kernel1(__global int* y,
  __read_only pipe int __attribute__((bsp)) c)
{
 int i=get_local_id(0);

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 int temp=0;
 read_bsp_pipe(c,&temp);
 y[i]=temp;
}
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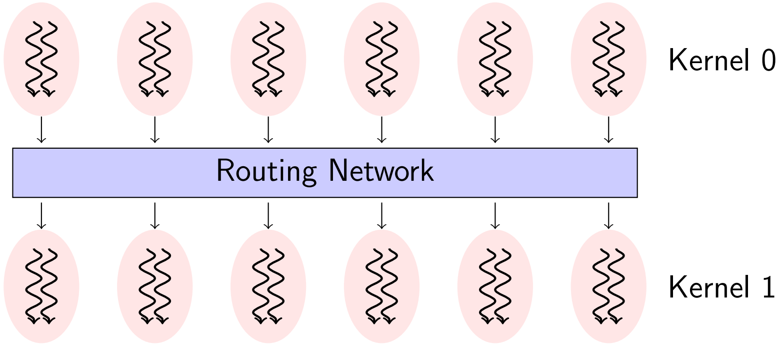
Message Routing between threads



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  - Potential implications on storage costs at destination
- Depending on bottleneck, optimize either logic or the network

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- BSP requires a new form of synchronization $\rightarrow$ probably analogous to `commit_pipe`
- BSP message-passing can be implemented using an FPGA NoC

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- TODO: Someone please make an OpenCL lexer for Pygments + LaTeX