GPU DAEMON
ROAD TO ZERO COST SUBMISSION

MICHAL MROZEK

ZBIGNIEW ZDANOWICZ

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Agenda

- Current OpenCL™ scheduling model
- GPU Daemon:
  - Instant Mode
  - Enqueue Mode
- Performance Data
- Efficient use of GPU Daemon patterns
- Summary

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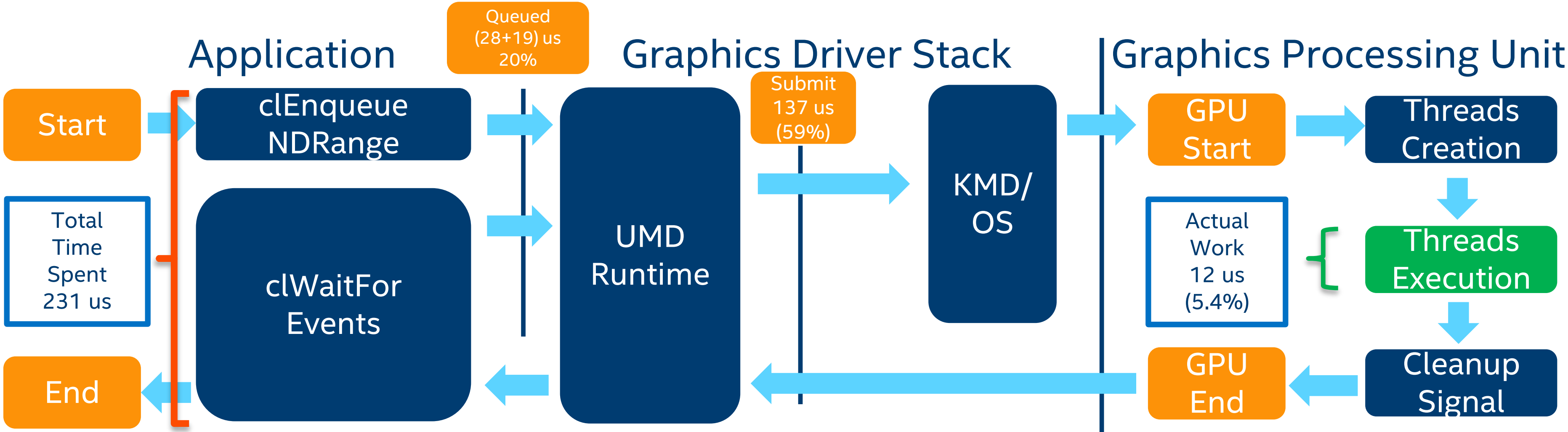
Current OpenCL™ scheduling model



Submission latencies	CPU Start to Queue	Queue to Submit	Submit to GPU Start	GPU Start to GPU End REAL WORK	GPU End To CPU End	Total
Subsequent enqueue	28	19	137	12	32	231

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Current OpenCL™ scheduling model

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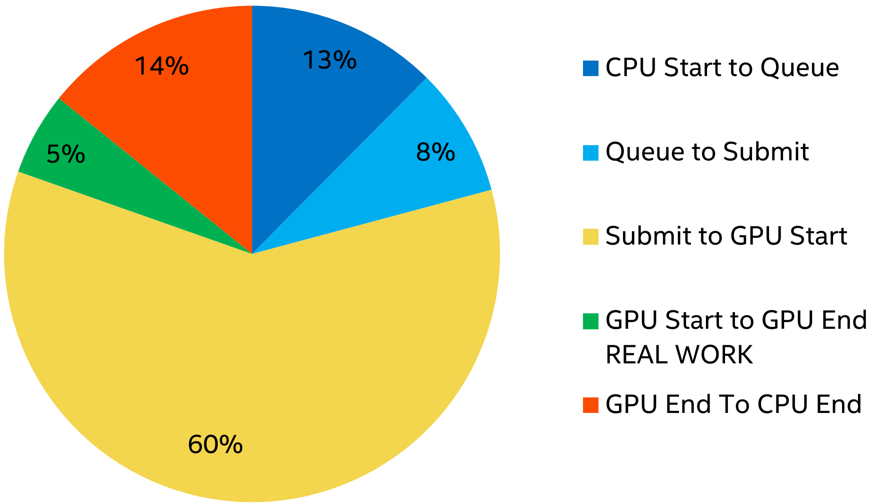

- Driver overhead is significant:
  - Not suitable for small kernels.
  - Not suitable for low latency scenarios.
- Submission is expensive:
  - Memory needs to be resident.
  - GPU threads are created & destroyed for each kernel.
- Why queue if I want to submit ?
  - No queue needed if 0 cost submission & completion.

Current scheduling model doesn't suit well for low latency / short workloads

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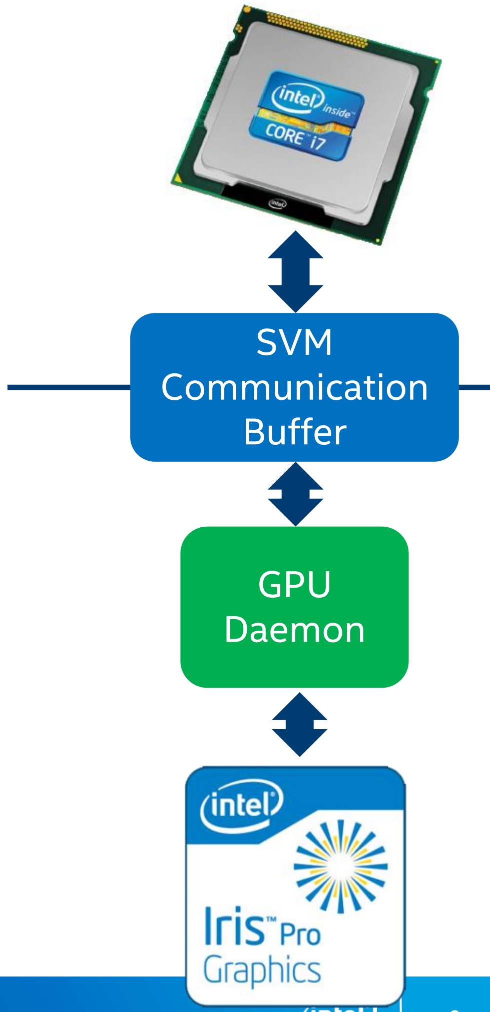
Introducing GPU Daemon

- GPU Daemon is a kernel launched from the host and later persistent on the GPU.
- It communicates with CPU using Fine-Grained Shared Virtual Memory with atomics.
- Persistency is achieved using various methods:
  - Instant Mode – loop within a kernel.
  - Enqueue Mode – self-enqueue utilizing device_enqueue.
- CPU communicates directly with active GPU threads bypassing driver stack.
- Whenever Daemon is no longer needed CPU sends “end” signal that will terminate GPU threads.



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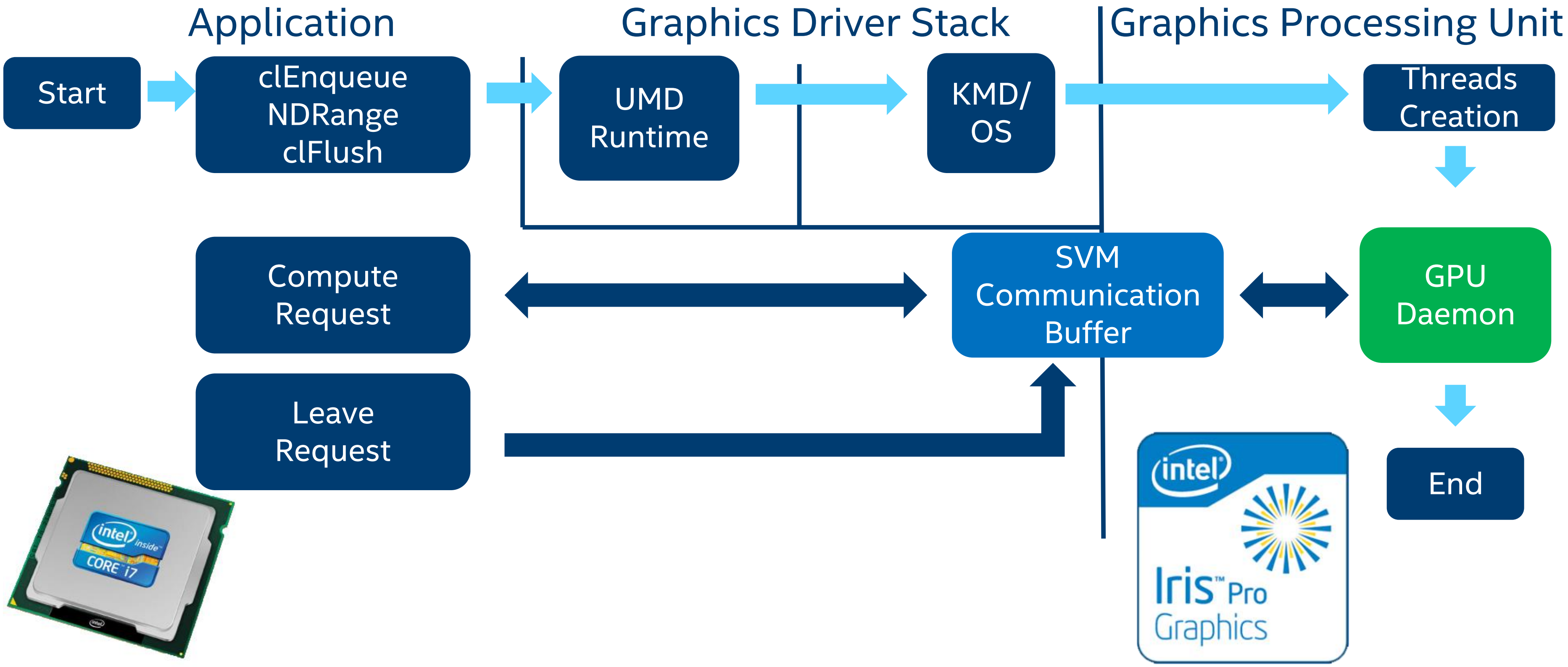
Introducing GPU Daemon – Instant Mode



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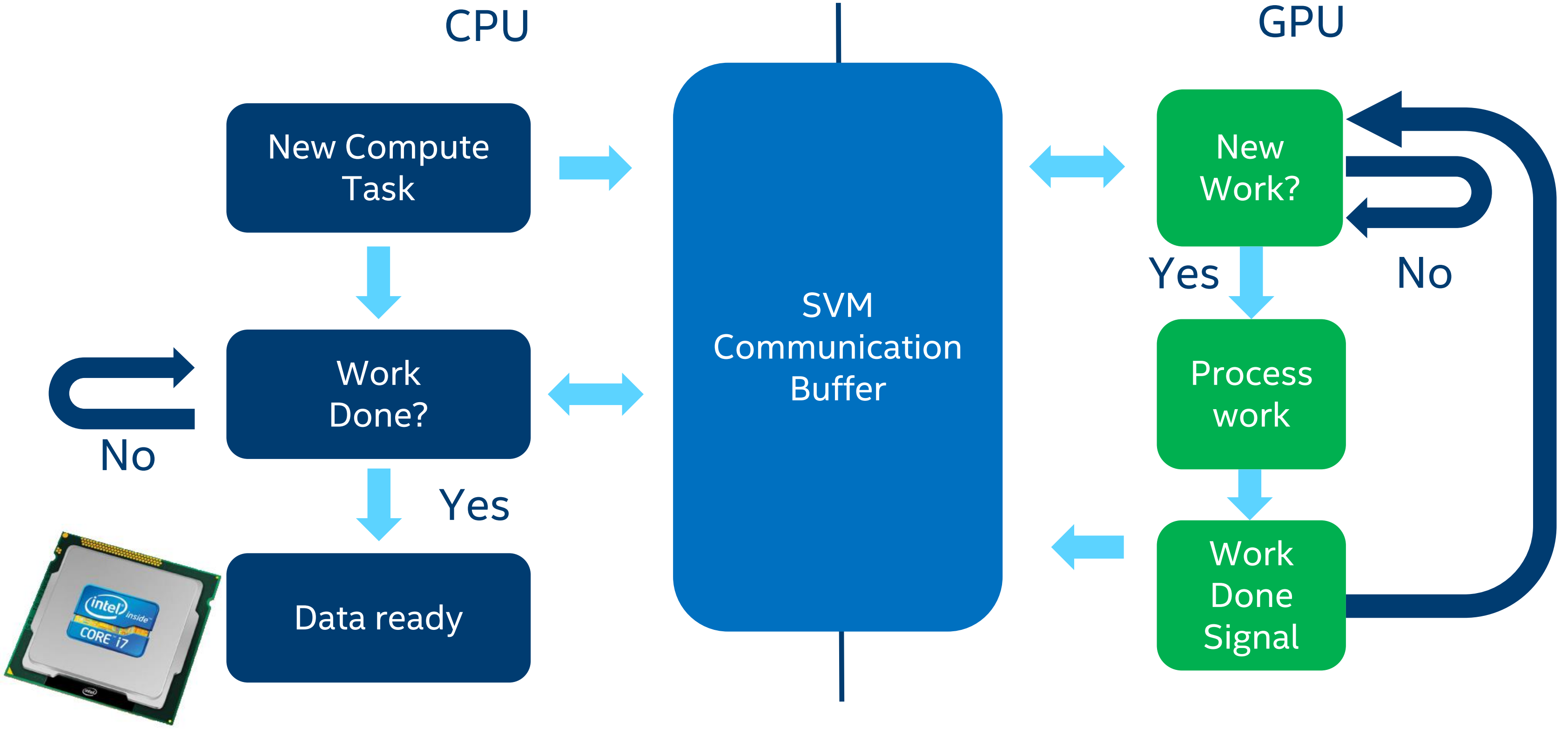
Instant Mode – tasks processing



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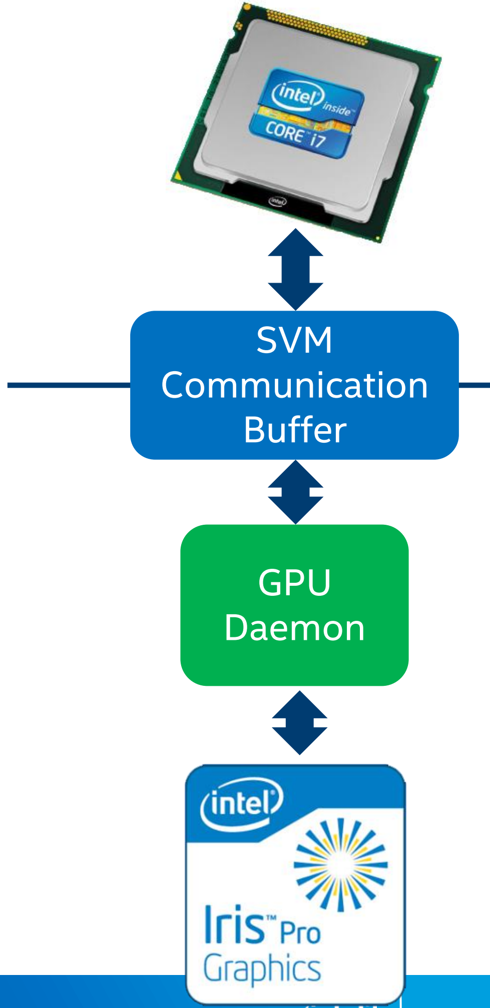
GPU Daemon in Enqueue mode

- Enqueue Mode allows various different transitions:
  - Utilizes device self-enqueue feature of OpenCL™ 2.0.
  - GPU can switch to Instant mode for direct submission.
  - GPU can enqueue traditional kernels without the need of host API interaction.
- Gives great flexibility in terms of possible options:
  - Whole host code can be transferred to the device.
  - Various Instant kernels may be dispatched, serving different compute algorithms.



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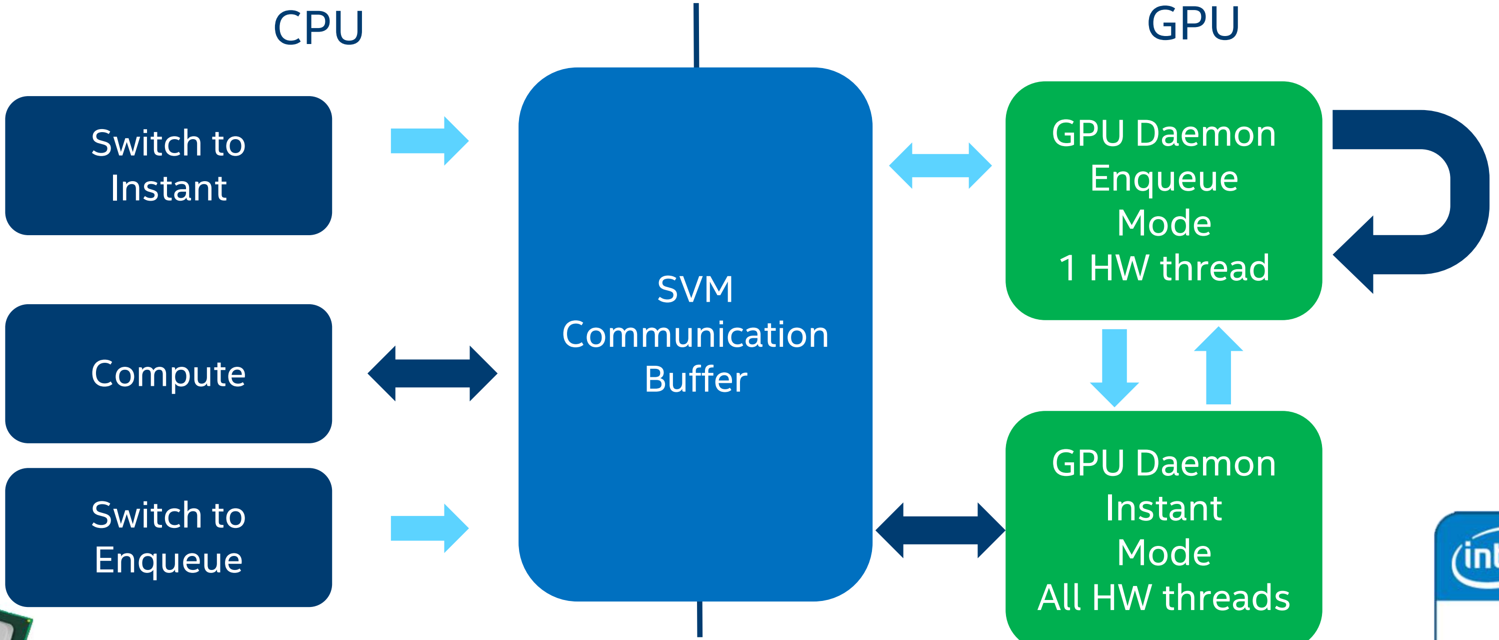
Introducing GPU Daemon – Enqueue mode



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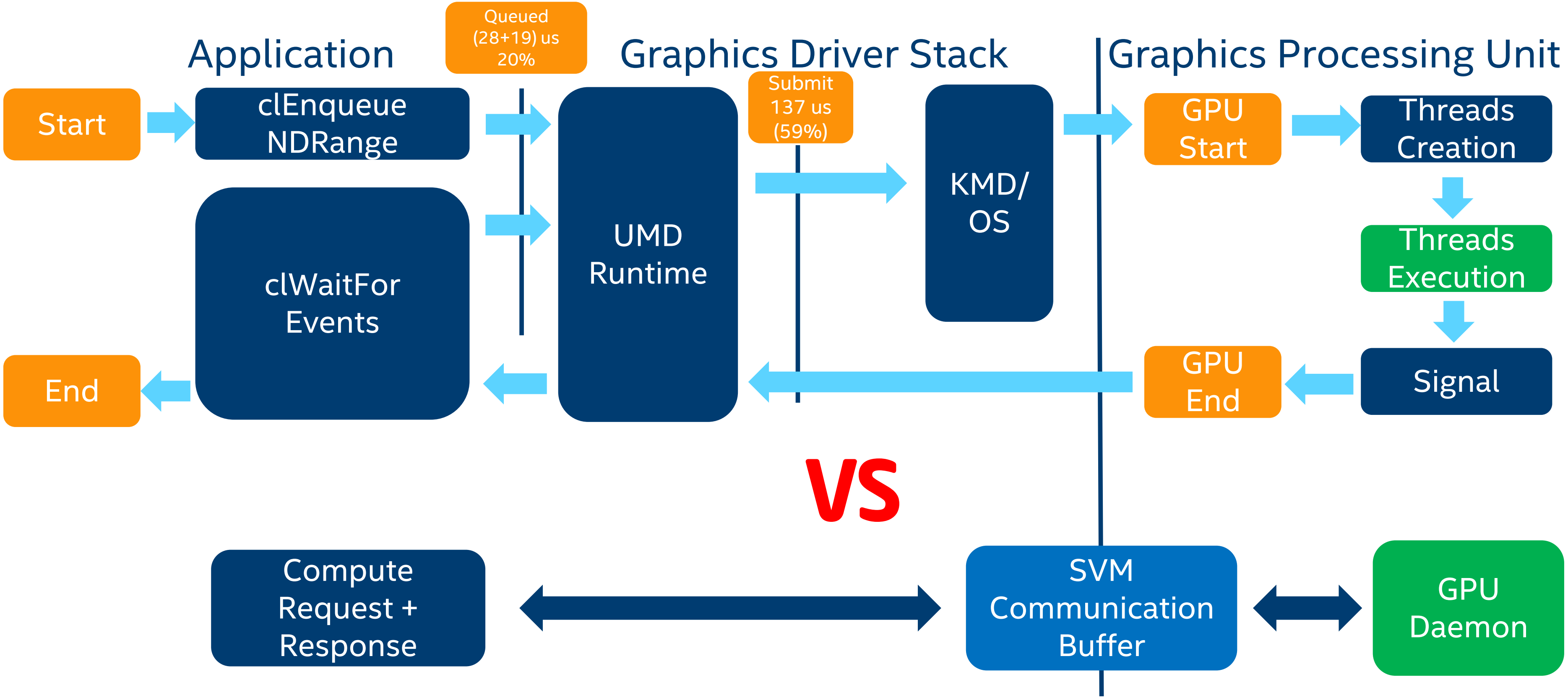
Model Comparison – classic vs GPU Daemon



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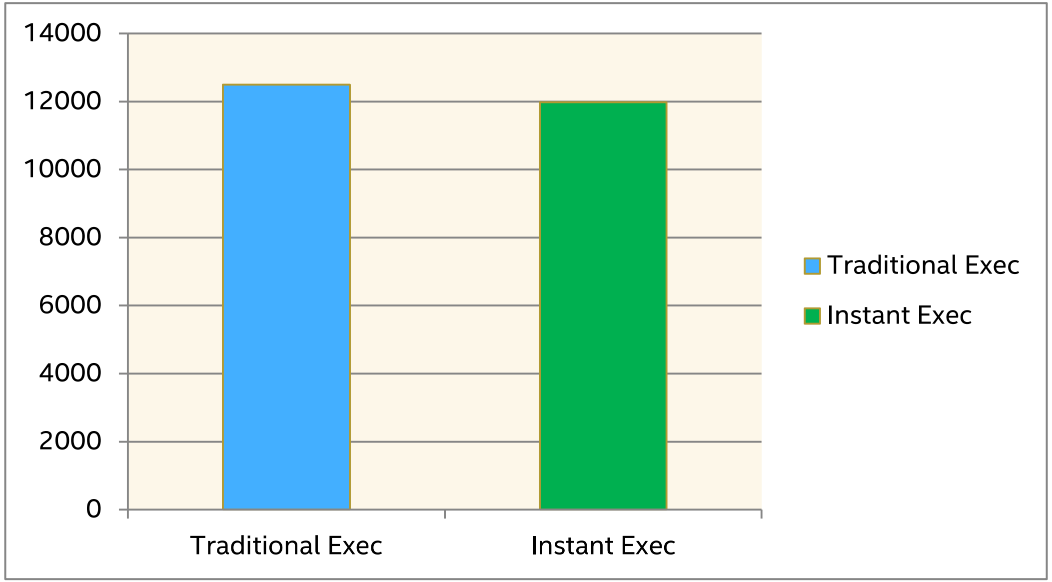
Kernel execution comparison (ns)



- Instant Mode Execution is faster than traditional enqueue (+5%):
  - No Thread Creation
  - No Thread Destruction
  - GPU boosted to high frequency
- This time includes CPU + GPU atomics communication cost for submission and completion.
- After work is done, threads are immediately ready for next submission.

No kernel execution overhead with CPU+GPU synchronization.

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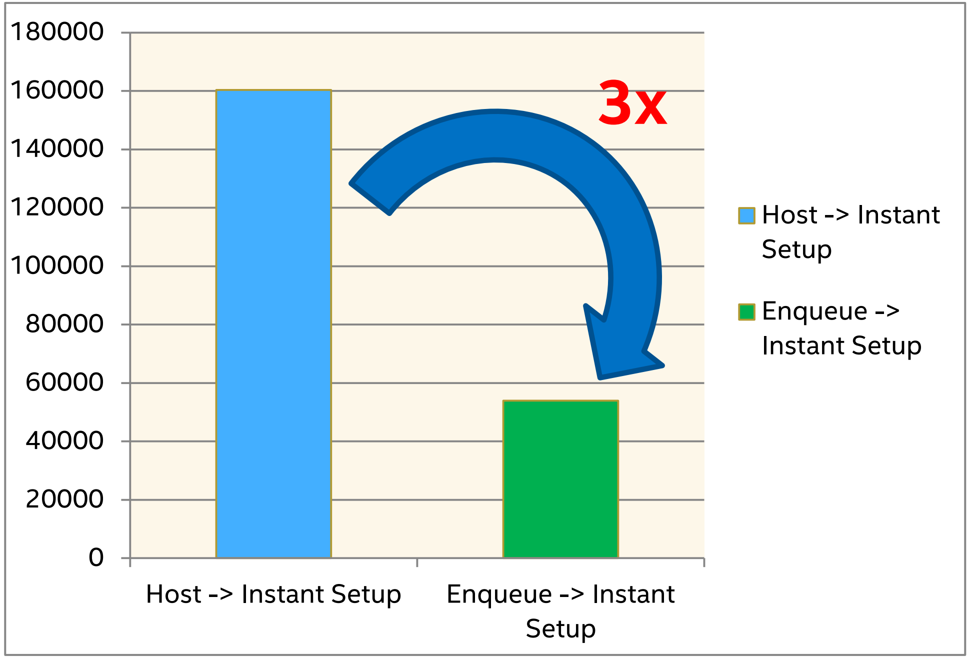
Mode Transition Latency (ns)



- Instant mode may be initiated from the host or from GPU Daemon in Enqueue Mode.
- Time needed to enter Instant Mode from the host is 160 us.
- Same operation from GPU Daemon being in Enqueue mode takes 58 us.
- Useful when multiple different instances of Instant kernels will be required.

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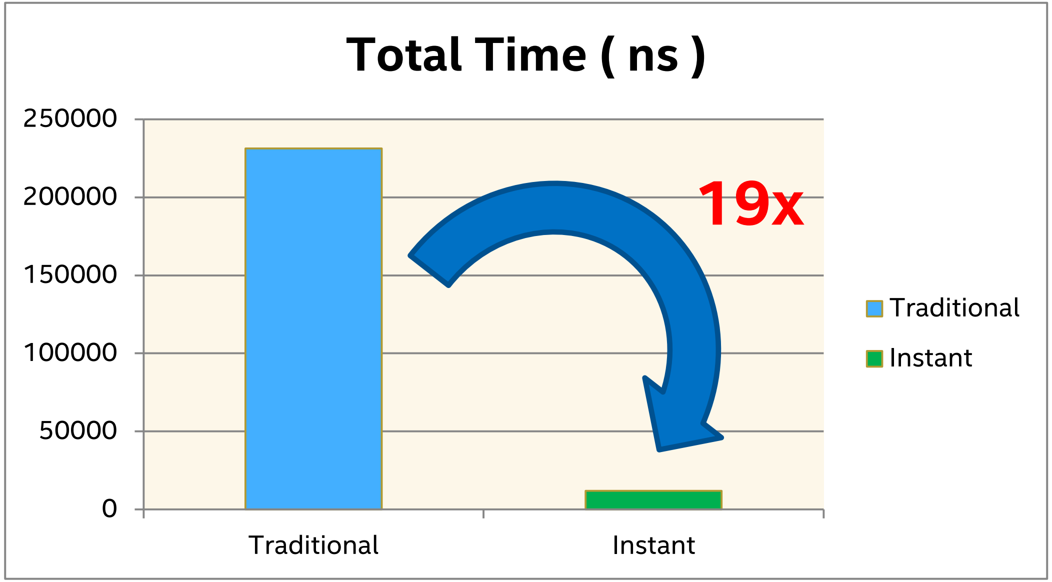
Model Comparison – Instant with active Daemon



- Time from start to completion of the compute task reduced **19 times** !
- This includes submission, processing and completion of compute tasks.
- All latencies are not present, immediate compute power available on demand.

GPU Daemon is a very efficient technique for zero cost submission & completion.

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Make sure you spawn all HW threads available

- Query Number of Execution Units using:

clGetDeviceInfo + CL_DEVICE_MAX_COMPUTE_UNITS

- Multiply it by number of hardware threads on each EU (typically 7, refer to device documents), this will give you total HW threads count, i.e. for Intel(R) HD Graphics 560:

24 * 7 = 168 Hardware Threads

- Obtain SIMD size of your kernel using (8,16,32):

clGetKernelWorkGroupInfo + CL_KERNEL_PREFERRED_WORK_GROUP_SIZE_MULTIPLE

- Compute global work size that will result in all threads being spawned:

Gws[0] = SIMDsize * NumberOfHwThreads = 32 * 168 = 5376

- Make sure your LWS is a multiple of SIMDsize.

- Make sure your GWS is a multiple of LWS.

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Play nicely with GPU

- Be cautious to not spawn more HW threads than device has.
- Choose Local Work Group Size that fits nicely into sub-slices:
  - Get familiar with https://software.intel.com/sites/default/files/managed/c5/9a/The-Compute-Architecture-of-Intel-Processor-Graphics-Gen9-v1d0.pdf
  - Make sure number of HW threads per sub-slice is a multiple of HW threads per wkg.
- When using SLM(Shared Local Memory) / barriers choose bigger workgroup sizes to maximize SLM re-use:
  - Take into consideration that SLM is limited, so GPU may not spawn threads because of lack of free resources.
  - There is 64 KB per sub-slice for all workgroups, so if each uses 16KB then only 4 may be executed concurrently on this sub-slice.
- When Daemon is not needed terminate it to save power.

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Be cautious with the amount of atomic operations

1) DON'T increment spin on every work-item:

```
__kernel Worker(__global int* pCommBuffer)
{
 __global atomic_int *atomicCommBuffer =
(__global volatile atomic_int*)pCommBuffer;

    atomic_fetch_add_explicit(
        &atomicCommBuffer[SPIN],
        1,
        memory_order_seq_cst,
        memory_scope_all_svm_devices );
    //do the work
}
```

1) DO Only single increment per thread

```
__kernel Worker(__global int* pCommBuffer)
{
    __global atomic_int *atomicCommBuffer =
(__global volatile atomic_int*)pCommBuffer;

    if( get_sub_group_local_id() == 0 )
    {
        atomic_fetch_add_explicit(
            &atomicCommBuffer[SPIN],
            1,
            memory_order_seq_cst,
            memory_scope_all_svm_devices );
     }
     //do the work
}
```

Implicit SIMD synchronization reduces the amount of atomics up to 32x.

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Or even better, synchronize on Workgroup basis

```
__private int Finish = 0;
__private int ReqPhase = 0;
//loop as long as you need to
while( Finish != 0 )
{
    //each work item needs to check for
    work
    ReqPhase = atomic_load_explicit(
    &atomicCommBuffer[PHASE],
    memory_order_seq_cst,
     memory_scope_all_svm_devices );
    //each work item needs to obtain
    flag
    Finish = atomic_load_explicit(
    &atomicCommBuffer[FINISH],
    memory_order_seq_cst,
     memory_scope_all_svm_devices);
    //do some work
}
```

```
//shared local memory keeps control variables
__local uint Finish;
__local uint ReqPhase;
ReqPhase = Finish = 0;
barrier( CLK_LOCAL_MEM_FENCE );
//setup done, now loop as long as you need to
while(1){
    //one work item checks for completion OR new work
    if(get_local_id(0) == 0 ) {
     ReqPhase= atomic_load_explicit( &SVMComm[PHASE],
     memory_order_seq_cst,memory_scope_all_svm_devices);
     Finish= atomic_load(&SVMComm[FINISH],
     memory_order_seq_cst,memory_scope_all_svm_devices);
     //obtain work info here and propagate to SLM
    }
    barrier( CLK_LOCAL_MEM_FENCE );
    //all work items are synchronized here
    if( Finish != 0 ) return;
    //do the work on all work items basing on SLM inputs
```

Atomic traffic reduced by the factor of workgroup size (up to 256x)

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GPU Daemon Instant mode – Thread Spawn

CPU

```
//SVM communication buffer
std::atomic<unsigned int>*pCommBuffer =
(std::atomic<unsigned int>*)pData;
size_t gws = m_NumberOfHWThreads *
kernelSIMD;
//use 4 HW threads per WKG to minimize
atomic traffic
size_t HWThreadsPerWKG = 4;
size_t lws = kernelSIMD * HWThreadsPerWKG;

clEnqueueNDRange("InstantKernel",gws,lws);
clFlush();

//wait before GPU is ready , each thread
will signal
while(pCommBuffer[SPIN] <
m_NumberOfHWThreads);
//if we are here it means that GPU is ready
for submissions on all HW threads
```

GPU

```
__kernel InstantKernel(global int* pCommBuffer){
//tell compiler we will need atomic operations
global atomic_int *SVMComm = (global volatile
atomic_int*)pCommBuffer;
//each HW thread notifies that it is ready
if(get_sub_group_local_id() == 0) {
    atomic_fetch_add_explicit(
        &SVMComm [SPIN],1,
        memory_order_seq_cst,
        memory_scope_all_svm_devices );
}
//initialize SLM to use it later for workgroup
communication
local int Finish;
local int ReqPhase;
ReqPhase = Finish = 0;
barrier( CLK_LOCAL_MEM_FENCE );
//setup done, we may enter polling mode
```

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GPU Daemon Instant mode – communication

CPU

```
//make sure atomics are used
std::atomic<unsigned int>*pCommBuffer =
(std::atomic<unsigned int>*)pData;

for(uint i = 0; i < iterations; i++) {
    //triger workload
    pCommBuffer[PHASE]= ++Phase;
    //wait before completion
    while(pCommBuffer[COMPLETE]
                < m_numWorkgroups);
    //data is ready GPU completed

    //re-init completion value for next iter
    pCommBuffer[COMPLETE] = 0;
}

//terminate Instant
pCommBuffer[FINISH] = 1;
```

GPU

```
uint Phase = 0;
while(1) {
if(get_local_id(0) == 0) {
    Finish = atomic_load(&SVMComm[FINISH]);
    ReqPhase = atomic_load(&SVMComm[PHASE]);
}
barrier( CLK_LOCAL_MEM_FENCE );
if(Finish != 0) return;
if(Phase < ReqPhase) {
    //do some work, increment Phase
    Phase++;
    //now signal completion
    barrier( CLK_GLOBAL_MEM_FENCE );
    if(get_local_id(0) == 0 ) {
        atomic_fetch_add_explicit(
        &SVMComm[COMPLETE],
        1, memory_order_seq_cst,
        memory_scope_all_svm_devices );}
}
```

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Summary

- GPU Daemon is a **very** efficient technique for direct submission.
  - Submission and completion driver overhead is eliminated.
  - Kernel execution is boosted.
- GPU Daemon offers various modes allowing very flexible application paradigms
  - Instant Mode for direct submission
  - Enqueue Mode whenever we need to switch between modes or enqueue other workloads that don't require direct submission
- Get familiar with https://software.intel.com/sites/default/files/managed/c5/9a/The-Compute-Architecture-of-Intel-Processor-Graphics-Gen9-v1d0.pdf

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