

Presentation

Developing Medical imaging application across GPU, FPGA, and CPU using oneAPI

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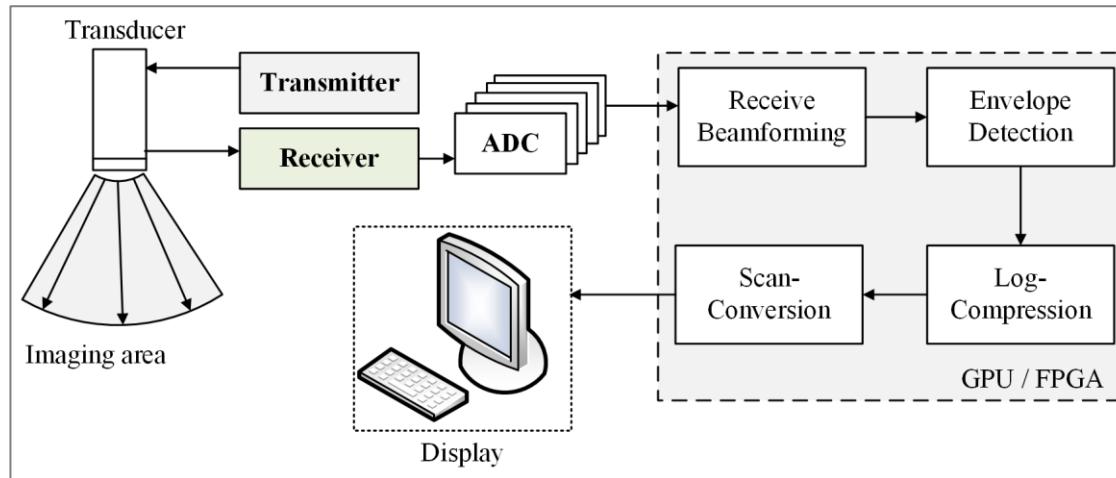
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- Beamforming implementation on FPGA
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Background

What is SUPRA and why we need it?

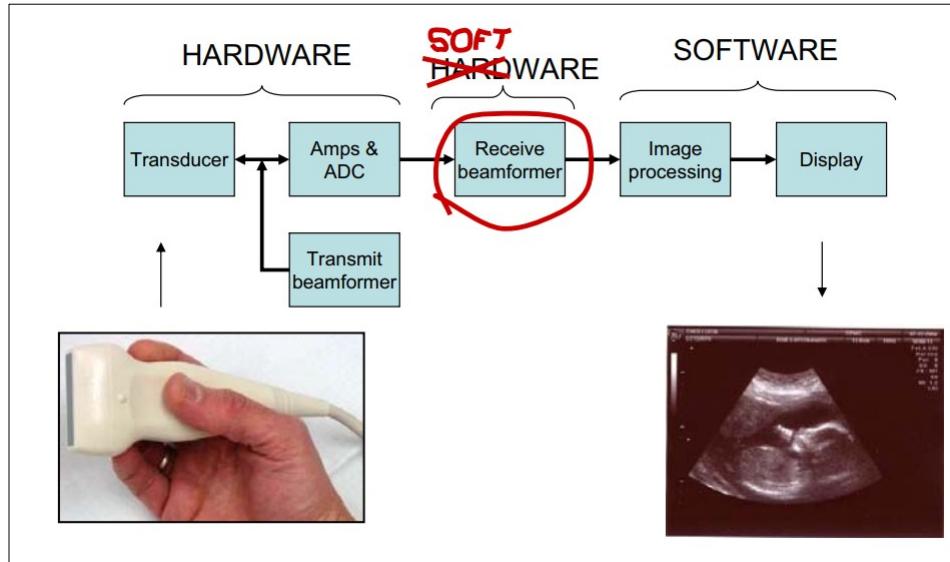
SUPRA is an open-source pipeline for fully software defined ultrasound processing.

- <https://github.com/IFL-CAMP/supra>



What is software beamforming?

SUPRA contains standard medical ultrasound software beamforming algorithms.



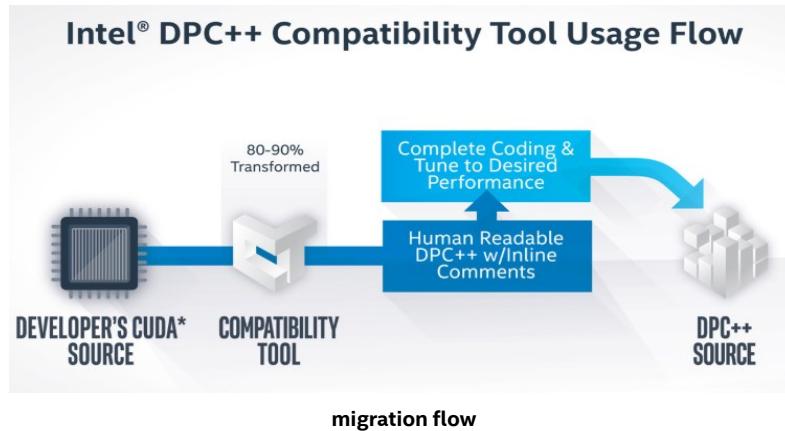
Software beamforming illustration.(Fig source: Lars Grønvold)

Intel's products in software beamforming :

- Core & Gen9 graphics, DG1, Arria 10 & Stratix 10, Intel oneAPI.

Code Migration

migration flow



- The Intel® DPC++ Compatibility Tool assists in migrating your existing CUDA code to Data Parallel C++ (DPC++) code
- DPC++ is based on ISO C++ and incorporates standard SYCL* and community extensions to simplify data parallel programming
- Inline comments help you finish writing and tuning your DPC++ code

OneAPI Version	Total num of migration place	Success migrated	Need modify	Accuracy
beta07	84	63	21	75%
golden	84	75	9	89%

SUPRA migration summary

File Type	*.cpp	*.cu	*.h
File num	1	4	23

num. of migrated file

Migration Command: `dpct --in-root= ./ --out-root= ./oneapi --extra-arg=-Isrc/SupraLib --extra-arg=-Isrc/SupraLib/Beamformer --extra-arg=-Isrc/SupraLib/utilities --extra-arg=-std=c++11 --extra-arg=-Wno-c++11-narrowing --extra-arg=-DHAVE_CUDA ./src/SupraLib/Beamformer/ScanConverter.cu ./src/SupraLib/Beamformer/HilbertFirEnvelope.cu ./src/SupraLib/Beamformer/LogCompressor.cu ./src/SupraLib/Beamformer/RxBeamformerCuda.cu ./src/SupraLib/ContainerFactory.cpp`



Migrated code APIs

Category	oneAPI APIs
Memory Management	<code>sycl::malloc_device()</code> <code>sycl::malloc_shared()</code> <code>sycl::free()</code> <code>sycl::malloc_host()</code> <code>sycl::queue.memcpy()</code> <code>Sycl::queue.memset()</code>
<code>sycl::queue</code>	<code>dpct::get_current_device().create_queue()</code> <code>dpct::get_default_queue()</code> <code>sycl::queue()</code> <code>sycl::queue.submit()</code> <code>sycl::queue.wait()</code>
Math	<code>sycl::sqrt(); sycl::floor(); sycl::fabs(); sycl::round()</code> <code>sycl::max(); sycl::min(); sycl::log10(); sycl::pow()</code>
Express Parallel	<code>sycl::nd_item<>; Sycl::nd_range<>; Sycl::range<></code> <code>sycl::id<>; Sycl::nd_item().get_local_range()</code> <code>sycl::nd_item().get_group()</code> <code>sycl::nd_item().get_local_id()</code>



Manually migration example

```
cuda → | → cudaEvent_t · m_creationEvent;  
#endif
```

1.

migrate

modify Remove the migrated `sycl::event` and `std::chrono` object

```
cudaSafeCall(cudaStreamCreateWithFlags(&(sm_streams[k]), cudaStreamNonBlocking));
```

2. migrate

modify

```
//cudaSafeCall(((sm_streams[k]) = dpct::get_current_device().create_queue()));  
sm_streams[k] = new sycl::queue(dpct::get_default_queue_wait().get_context(), dpct::get_default_queue_wait().get_device(), property_list);
```



Manually migration example

```
template <typename InputType, typename OutputType>
shared_ptr<Container<OutputType>> LogCompressor::compress(const shared_ptr<const Container<InputType>>& inImageData, vec3s size,
+ double dynamicRange, double scale, double inMax)
{
    size_t width = size.x;
    size_t height = size.y;
    size_t depth = size.z;

    auto pComprGpu = make_shared<Container<OutputType>>(LocationGpu, inImageData->getStream(), width*height*depth);

    OutputType outMax;
    if (std::is_integral<OutputType>::value)
    {
        outMax = std::numeric_limits<OutputType>::max();
    }
    else if (std::is_floating_point<OutputType>::value)
    {
        outMax = static_cast<OutputType>(255.0);
    }

    thrustLogcompress<InputType, OutputType, WorkType> c(pow(10, (dynamicRange / 20)), static_cast<InputType>(inMax), outMax, scale);
    thrust::transform(thrust::cuda::par.on(inImageData->getStream()), inImageData->get(), inImageData->get() + (width*height*depth),
+ pComprGpu->get(), c);
    cudaSafeCall(cudaPeekAtLastError());

    return pComprGpu;
}
```

```
template <typename InputType, typename OutputType>
shared_ptr<Container<OutputType>> LogCompressor::compress(const shared_ptr<const Container<InputType>>& inImageData,
+ vec3s size, double dynamicRange, double scale, double inMax)
{
    size_t width = size.x;
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    size_t depth = size.z;

    auto pComprGpu = make_shared<Container<OutputType>>(LocationGpu, inImageData->getStream(), width * height * depth);

    OutputType outMax;
    if (std::is_integral<OutputType>::value)
    {
        outMax = std::numeric_limits<OutputType>::max();
    }
    else if (std::is_floating_point<OutputType>::value)
    {
        outMax = static_cast<OutputType>(255.0);
    }

    thrustLogcompress<InputType, OutputType, WorkType> c(
+ sycl::pow((float)10, (float)(dynamicRange / 20)), static_cast<InputType>(inMax), outMax, scale);

    auto in_data = inImageData->get();
    auto out_data = pComprGpu->get();
    inImageData->getStream()->wait();

    //static long call_count = 0;
    //static std::chrono::duration<double, std::milli> total_duration(0);

    sycl::event e_log = inImageData->getStream()->submit([&](sycl::handler &agh) {
        agh.parallel_for<>(sycl::range<1>(width * height * depth), [=](sycl::id<1> idx) {
+         out_data[idx] = c(in_data[idx]);
        });
    });
}
```

DPCT tool can't migrate CUDA thrust library related code, so it must be rewritten using oneAPI model.



Migration success example

```
cudaSafeCall(cudaMalloc((void**)&buffer, numBytes));
```

```
cudaSafeCall((buffer = (uint8_t*)sycl::malloc_device(numBytes, dpct::get_current_device(), dpct::get_default_context())), 0));
```

```
cudaSafeCall(cudaMallocManaged((void**)&buffer, numBytes));
```

```
cudaSafeCall((buffer = (uint8_t*)sycl::malloc_shared(numBytes, dpct::get_current_device(), dpct::get_default_context())), 0));
```

```
cudaSafeCall(cudaMallocHost((void**)&buffer, numBytes));
```

```
cudaSafeCall((buffer = (uint8_t*)sycl::malloc_host(numBytes, dpct::get_default_context())), 0));
```

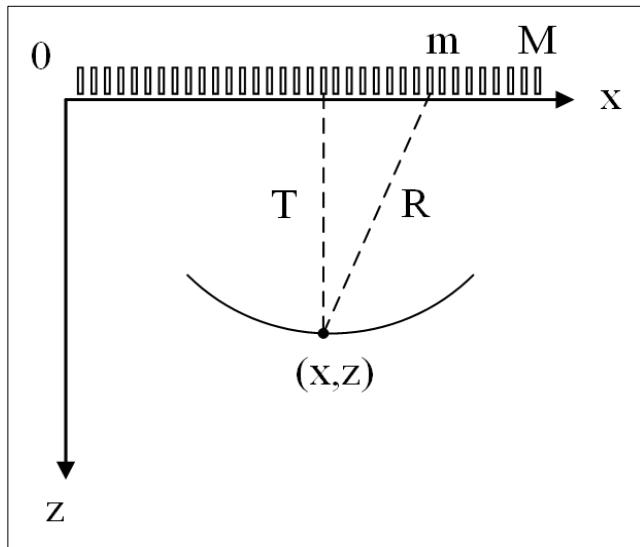
Memory allocate related function were successfully migrated.



Table 3 migrated CUDA API summary

Beamforming Optimization on GPU

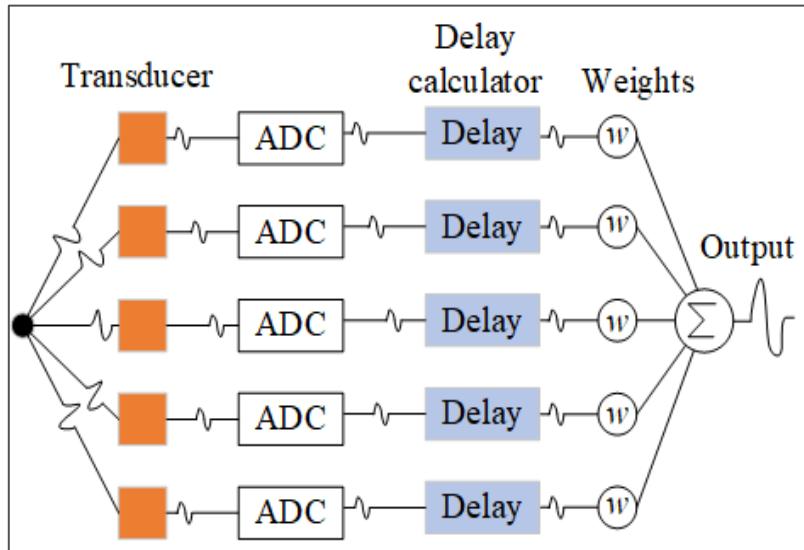
Beamforming(Delay and Sum) introduction



Geometrical illustration of the pulse-echo process

$$\Delta t = (T + R)/c_0$$

c_0 : the speed of ultrasound travel in the body.

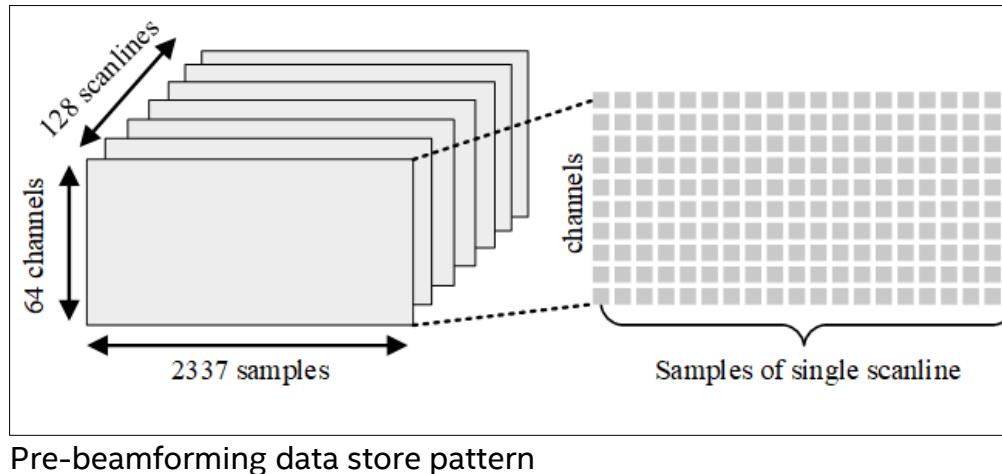


Delay and sum algorithm illustration

Beamforming introduction

Suppose pre-beamformed data: 128 scanlines. 64 channels. 2337 samples. It is arranged in a 3-D data structure: rf_data[scanline][channel][sample].

Memory required to store pre-beamformed data per image frame is:
 $(128 * 64 * 2334 * 2)$ bytes = 36.5 MB



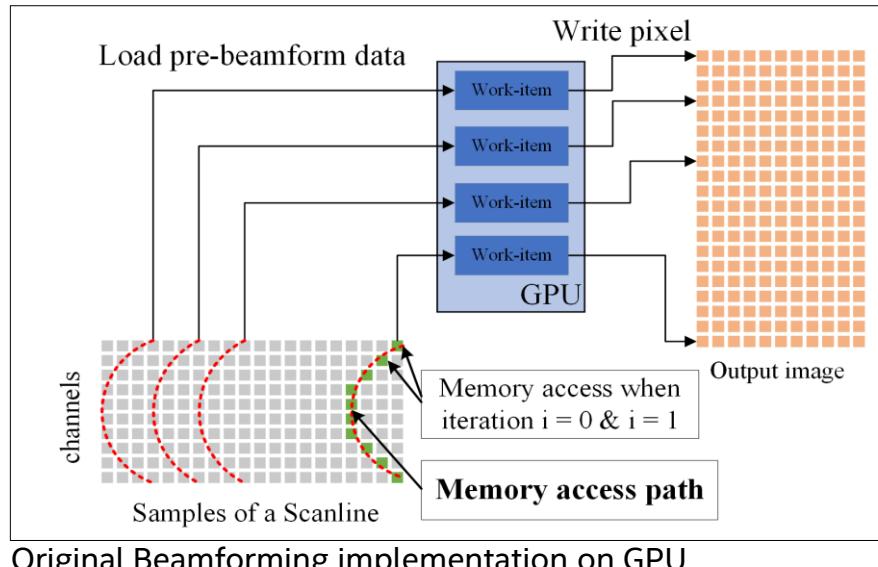
Beamforming algorithm implementation in single thread

Input: 3 dimensional pre-beamformed rf_data[numScanline][numSample][numChannel].

Output: A single frame image.

```
1  for k = 0 -> (numScanline - 1) do           Iteration In output image column direction.  
2      Read rf_data of k-th scanline;          Can be calculate Independently.  
3      for i = 0 -> (numSample - 1) do         Iteration in output image row direction.  
4          for j = 0 -> (numChannel - 1) do      Can be calculate Independently.  
5              calculate delay of j-th channel.  
6              load data and perform weighting.  
7              Sum all channels.  
8          write pixel value.  
9      Save and display image.
```

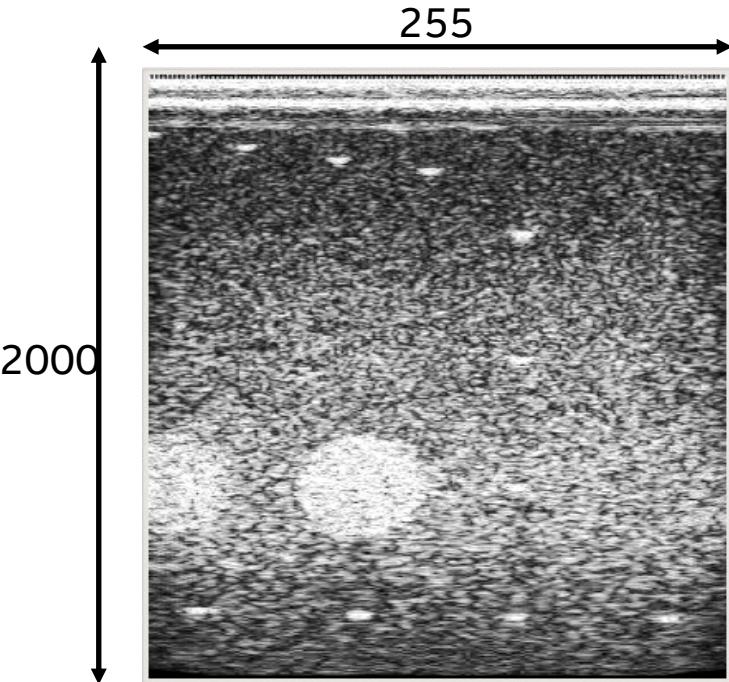
Beamforming implementation in parallel on GPU



Optimization #1

The optimization is in RxBeamformerCuda.dp.cpp and RxSampleBeamformerDelayAndSum.h file.

Function `rxBeamformingDTSPACEKernel` and `sampleBeamfor2D` are optimized.



Optimization idea:

CUDA: Each thread calculates a point;
every point iterates 64 times.

oneAPI: each thread load 2 points in
vertical direction, Iterates 8 times.

Optimization #1 oneAPI code

In RxBeamformerCuda.cu the function been called; the return value is a **float**.

In sampleBeamform2D function, calculate single point each call. The for loop at least iterates 64 times.

```
#pragma unroll
for (int i = 0; i < row_size; i++) {
    LocationType invMaxElementDistance = 1 / sycl::min(aDT[i], maxElementDistance);
    sInterp[i] = SampleBeamformer::template vec_sampleBeamform2D<interpolateRfLines, RFType, float, LocationType>(txParams, RF, numTransducerElements,
    numReceivedChannels, numTimesteps, x_elemsDT, scanline_x, dirX, dirY, dirZ, aDT[i], d[i], invMaxElementDistance, speedOfSound, dt, additionalOffset,
    windowFunction, mdataGpu);
}

template <bool interpolateRfLines, typename RFType, typename ResultType, typename LocationType>
static ResultType vec_sampleBeamform2D( ScanlineRxParameters3D::TransmitParameters txParams, const RFType* RF, uint32_t numTransducerElements, uint32_t numReceivedChannels,
    uint32_t numTimesteps, const LocationType* x_elemsDT, LocationType scanline_x, LocationType dirX, LocationType dirY, LocationType dirZ, LocationType aDT,
    LocationType depth, LocationType invMaxElementDistance, LocationType speedOfSound, LocationType dt, int32_t additionalOffset,
    const WindowFunctionGpu* __restrict__ windowFunction, const float* mdataGpu
)
{
    const int VEC_SIZE = 8;
    float sampleAccum = 0.0f;
    float weightAccum = 0.0f;
    int numAdds = 0;
    LocationType initialDelay = txParams.initialDelay;
    uint32_t txScanlineIdx = txParams.txScanlineIdx;

    for (int32_t elemIdxX = txParams.firstActiveElementIndex.x; elemIdxX < txParams.lastActiveElementIndex.x; elemIdxX += VEC_SIZE)
    {
        sycl::vec<int, VEC_SIZE> channelIdx;
        sycl::vec<LocationType, VEC_SIZE> x_elem; } sycl::vec<float, 8>

        #pragma unroll
        for (int i = 0; i < VEC_SIZE; i +=2) {
            channelIdx[i] = (elemIdxX + i) % numReceivedChannels;
            channelIdx[i+1] = (elemIdxX + i + 1) % numReceivedChannels;
            x_elem[i] = x_elemsDT[elemIdxX + i];
            x_elem[i + 1] = x_elemsDT[elemIdxX + i + 1];
        }
        sycl::vec<float, VEC_SIZE> sample;
        sycl::vec<int, VEC_SIZE> mask = (sycl::fabs(x_elem - scanline_x) <= aDT);
        /*sycl spec1.2.1 mentioned: true return -1, false return 0*/
        mask *= -1;
        numAdds += utils<int, VEC_SIZE>::add_vec(mask); }
```

Use mask

Source code: supra/src/SupraLib/Beamformer/ RxSampleBeamformerDelayAndSum.h



Optimization #2

Another optimization in BeamformingNode is directly move into kernel function rather than using function call.

```
sycl::vec<float, VEC_SIZE> weight = windowFunction->get_vec((x_elem - scanline_x) * invMaxElementDistance);  
  
inline sycl::vec<ElementType, VEC_SIZE> get_vec(sycl::vec<float, VEC_SIZE> relativeIndex) const  
{  
    sycl::vec<float, VEC_SIZE> relativeIndexClamped =  
        sycl::min(sycl::max(relativeIndex, -1.0f), 1.0f);  
    sycl::vec<float, VEC_SIZE> absoluteIndex =  
        m_scale * (relativeIndexClamped + 1.0f);  
    sycl::vec<int, VEC_SIZE> int_absoluteIndex = absoluteIndex.convert<int, sycl::rounding_mode::automatic>();  
  
    sycl::vec<float, VEC_SIZE> v(0);  
    #pragma unroll  
    for(int i = 0; i < VEC_SIZE; i++) {  
        int index = int_absoluteIndex[i];  
        v[i] = m_data[index]; m_data is a private member in class WindowFunctionGpu.  
    }  
    return v;  
}
```

Source code: supra/src/SupraLib/Beamformer/WindowFunction.cpp

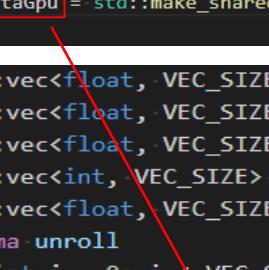
Before optimization, fetch data from windowFcuntion->m_data.



Optimization #2

Another optimization in BeamformingNode is directly move into kernel function rather than using function call.

```
// use gRawData->getStream().copy(data.to.GPU)
auto mdataGpu = std::make_shared<Container<float>>(ContainerLocation::LocationGpu, gRawData->getStream(), m_windowFunction->m_data);
```



```
sycl::vec<float, VEC_SIZE> relativeIndex = (x_elem - scanline_x) * invMaxElementDistance;
sycl::vec<float, VEC_SIZE> relativeIndexClamped = sycl::min(sycl::max(relativeIndex, -1.0f), 1.0f);
sycl::vec<float, VEC_SIZE> absoluteIndex = windowFunction->m_scale * (relativeIndexClamped + 1.0f);
sycl::vec<int, VEC_SIZE> absoluteIndex_int = absoluteIndex.convert<int, sycl::rounding_mode::automatic>();
sycl::vec<float, VEC_SIZE> weight;
#pragma unroll
for (int i = 0; i < VEC_SIZE; i += 2) {
    weight[i] = mdataGpu[absoluteIndex_int[i]];
    weight[i + 1] = mdataGpu[absoluteIndex_int[i + 1]];
}

//weightAcum += weight;
//numAddrs++;
weight *= mask.convert<float, sycl::rounding_mode::automatic>();
weightAcum += utils<float, VEC_SIZE>::add_vec(weight);
```

m_data was copied to mdataGpu before the queue->submit() call, then mdataGpu was directly passed to kernel function. For data copy, change m_data in WindowFunctionGpu to public.

Source code: supra/src/SupraLib/Beamformer/RxSampleBeamformerDelayAndSum.h

After optimization, fetch data from mdataGpu, mdataGpu was directly pass to kernel function



Optimization #2

GPU Compute/Media Hotspots (preview) GPU Compute/Media Hotspots (preview) ▾

Analysis Configuration Collection Log Summary Graphics

Architecture Diagram Platform

The diagram illustrates the system architecture. On the left, the GPU section shows the GPU Execution Units Array (Active: 96.1%, Stalled: 3.7%, Idle: 0.2%, 2M Threads/s), Sampler (Busy: 0.0%, Bottleneck: 0.0%), L1 and L2 caches, and SLM (2e+8 Misses/s). The L3 cache (2e+8 Misses/s) has a miss ratio of 16.2%. Data flows from the GPU to the Uncore (LLC, DRAM) and System (DRAM) via GTI. The CPU section shows utilization at 39.3%. A double-headed arrow connects the GPU and CPU sections.

Grouping: Computing Task

Computing Task	Work Size		Computing Task				Data Transferred			EU Array	
	Global	Local	Total Time	Average Time	Instance Count	SIMD Width	SVM Usage Type	Size	Total, GB/sec	Active	Stalled
_ZTSZNNsupra13LogCompressor8compressIfEESt1	510000		0.070s	0.000s	370	32		0 B	0.000	50.4%	25.9%
_ZTSZNNsupra18libcurlFeEnvelope10demodulateff	256 x 2000 x 1	16 x 8 x 1	0.855s	0.002s	370	16		0 B	0.000	66.7%	32.4%
_ZTSZNNsupra24nBeamformingDTspaceCudaNS_2	255 x 2048 x 1	1 x 256 x 1	6.995s	0.019s	370	16		0 B	0.000	96.1%	3.7%
_ZTSZNNsupra13ScanConverter7convertIfEESt10sh	1680 x 2000 x 1	16 x 8 x 1	1.063s	0.003s	368	32		0 B	0.000	17.6%	81.5%
cEnqueueMapBuffer			0.025s	0.000s	370			179 MB	7.485	0.0%	0.0%
[Outside any task]			0s							0.4%	1.6%

Before optimization

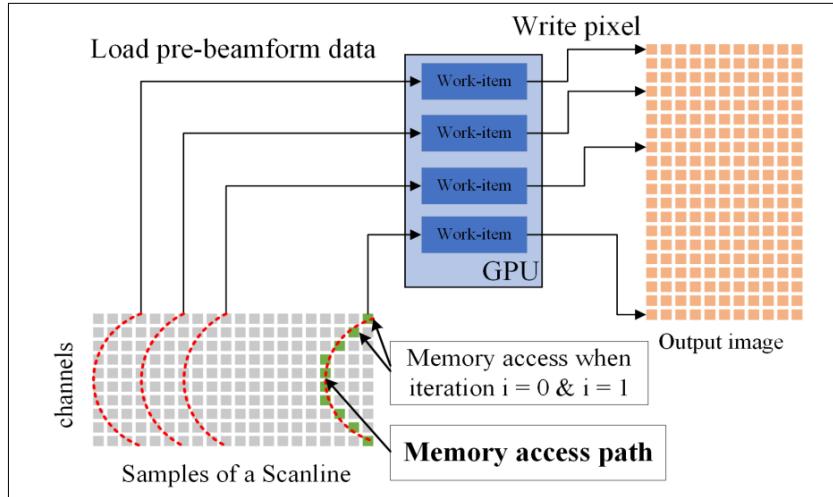
After optimization

Grouping: Computing Task

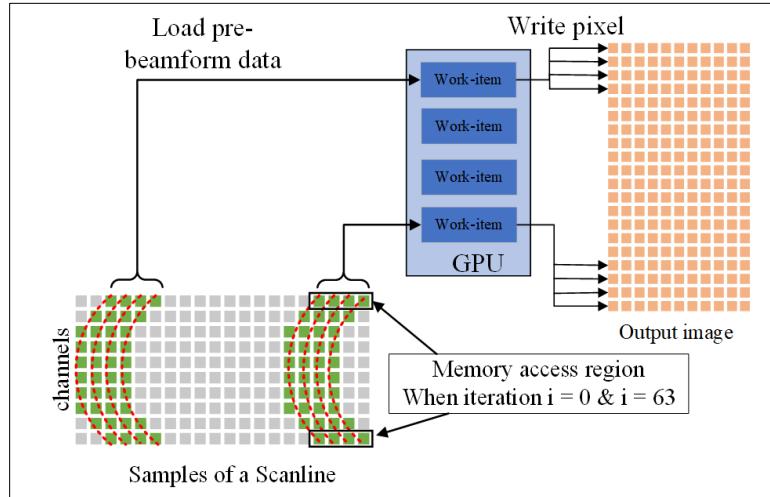
Computing Task	Work Size		Computing Task				Data Transferred			EU Array	
	Global	Local	Total Time	Average Time	Instance Count	SIMD Width	SVM Usage Type	Size	Total, GB/sec	Active	Stalled
_ZTSZNNsupra13LogCompressor8compressIfEESt1	510000		0.055s	0.000s	249	32		0 B	0.000	53.3%	26.0%
_ZTSZNNsupra18libcurlFeEnvelope10demodulateff	256 x 2000 x 1	16 x 8 x 1	0.702s	0.003s	249	16		0 B	0.000	68.4%	30.6%
_ZTSZNNsupra24nBeamformingDTspaceCudaNS_2	255 x 1024 x 1	1 x 256 x 1	2.767s	0.011s	250	8		0 B	0.000	79.9%	26.7%
_ZTSZNNsupra13ScanConverter7convertIfEESt10sh	1680 x 2000 x 1	16 x 8 x 1	0.717s	0.003s	248	32		0 B	0.000	19.2%	79.8%
cEnqueueMapBuffer			0.017s	0.000s	250			121 MB	7.540	0.0%	0.0%
[Outside any task]			0s							0.4%	1.5%



Using ESIMD to optimize beamforming



Original Beamforming implementation on GPU



Optimized Beamforming implementation on GPU

Beamforming implementation on FPGA

SUPRA on Intel FPGA Arria 10

SUPRA Node	oneAPI (ms) UHD630	oneAPI (ms) Arria 10
RxBeamforming	9.24	5.94↓ (Max)
HilbertFirEnvelope	1.50	2.61
LogCompressor	0.27	0.34
ScanConverter	2.65	5.66
Total	13.66	

SUPRA on FPGA has been tested on DevCloud, a Jupyter notebook provided to quick build and run.

The screenshot shows a Jupyter Notebook environment on a DevCloud instance. The left sidebar displays a file tree for a 'Supra' directory containing various build scripts and configuration files. The main area shows a code cell with Python code for generating four subplots. The code imports necessary libraries (Image, glob, plt, mpimg, time) and sets up a figure. It defines paths for four image files ('RxBeamformer', 'HilbertFirEnvelope', 'LogCompressor', 'ScanConverter') and iterates through them to create a 2x2 grid of plots. Each plot is a grayscale image with axes ranging from 0 to 350. The plots are titled 'Beamformer', 'HilbertFirEnvelope', 'LogCompressor', and 'ScanConverter'. Below the plots, a status bar indicates 'Saving completed'.

```
[4]: from IPython.display import Image
import glob
import matplotlib.pyplot as plt
import matplotlib.image as mpimg
import time
%matplotlib inline

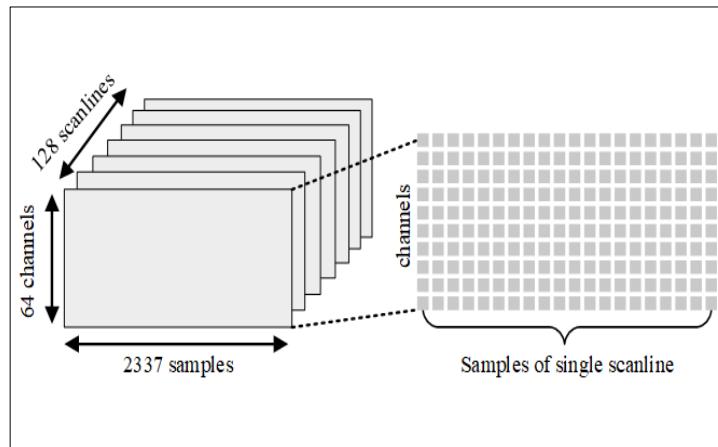
rows = 1
cols = 4
axes = []
fig = plt.figure(figsize=(15,8))

images_path = ["./emu_build/RxBeamformer/", "./emu_build/HilbertFirEnvelope/",
               "./emu_build/LogCompressor", "./emu_build/ScanConverter/"]
images_title = ["Beamformer", "HilbertFirEnvelope", "LogCompressor", "ScanConverter"]

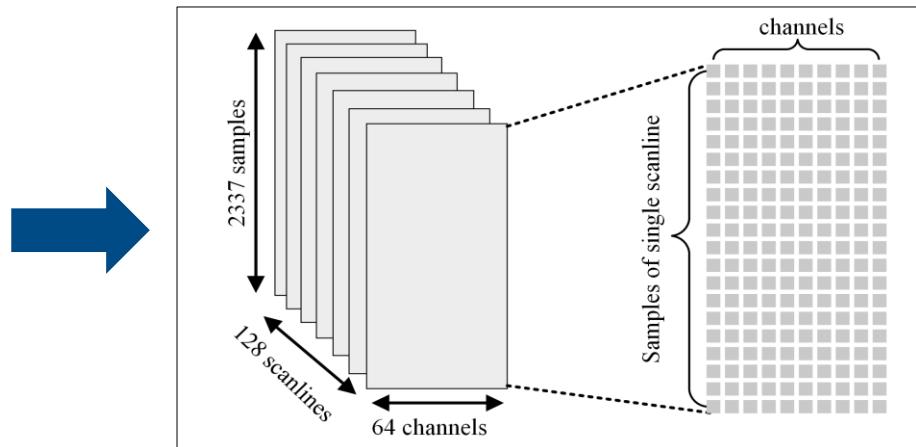
for img_index in range(8):
    for sub_img_index in range(4):
        img_path = images_path[sub_img_index] + str(img_index + 1) + '.png'
        axes.append(fig.add_subplot(rows, cols, sub_img_index+1))
        subplot_title = images_title[sub_img_index]
        axes[-1].set_title(subplot_title)
        img = mpimg.imread(img_path)
        plt.imshow(img, "gray")
    fig.tight_layout()
plt.show()
```

Link: https://gitlab.devtools.intel.com/qwang12/ultrasound-emu/-/tree/intelfpga_beta10

Beamforming on the FPGA

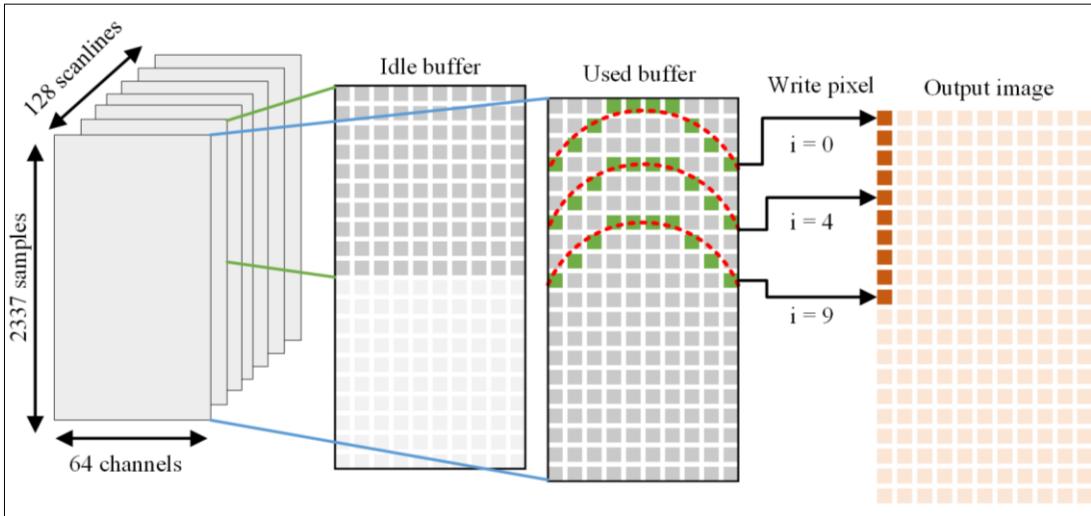


Original pre-beamformed data store pattern



Shuffled pre-beamformed data store pattern

Beamforming on the FPGA



```
Initial 2 local buffers, each contains a scanline data:  
rf_data_1[numSamples][numChannels]  
rf_data_2[numSamples][numChannels]  
1 for i = 0 --> number of Beamformed Image pixel do  
2   Calculate pixel index (r, c);  
3   Calculate depth according to r;  
4   Load next scanline data to rf_data_1 or rf_data_2;  
5   Fetch scanline parameters according to c;  
6   for j = 0 --> number of channels do  
7     if channel data inside window then  
8       fetch weight data according to channel;  
9       Calculate delay according to channel;  
10      Fetch RF data according to delay for jth channel;  
11    end  
12  end  
13  Sum weighted RF data for all channels;  
14  Write value to beamformed image buffer;  
15 end
```

Beamforming algorithm on FPGA

Beamforming implementation on FPGA

FPGA code: intelfpga-devcloud-golden/SupraLib/Beamformer/ RxBeamformerCuda.dp.cpp

Code Sample for FPGA

```
379 template <typename InputType, typename OutputType, typename WeightType, typename IndexType>
380 void scanConvert2D(
381     uint32_t numScanlines,
382     uint32_t numSamples,
383     uint32_t width,
384     uint32_t height,
385     const uint8_t * __restrict__ mask,
386     const IndexType * __restrict__ sampleIdx,
387     const WeightType * __restrict__ weightX,
388     const WeightType * __restrict__ weightY,
389     const InputType * __restrict__ scanlines,
390     OutputType * __restrict__ image,
391     sycl::nd_item<3> item_ct1)
392 {
393     vec2T<uint32_t> pixelPos{
394         item_ct1.get_local_range().get(2) * item_ct1.get_group(2) +
395         item_ct1.get_local_id(2),
396         item_ct1.get_local_range().get(1) * item_ct1.get_group(1) +
397         item_ct1.get_local_id(1); //@@suppress("Symbol is not resolved")
398         item_ct1.get_local_id(0); //@@suppress("Field cannot be resolved")
399     }
400     if (pixelPos.x < width && pixelPos.y < height)
401     {
402         IndexType pixelIdx = pixelPos.x + pixelPos.y * width;
403         float val = 0;
404         if (mask[pixelIdx])
405         {
406             IndexType sIdx = sampleIdx[pixelIdx];
407             WeightType wX = weightX[pixelIdx];
408             WeightType wY = weightY[pixelIdx];
409             val = (1 - wY) * ((1 - wX) * scanlines[sIdx] +
410                 wX * scanlines[sIdx + 1]) +
411                 wY * ((1 - wX) * scanlines[sIdx + numScanlines] +
412                 wX * scanlines[sIdx + 1 + numScanlines]);
413             image[pixelIdx] = clampCast<OutputType>(val);
414         }
415     }
416 }
417 }
```

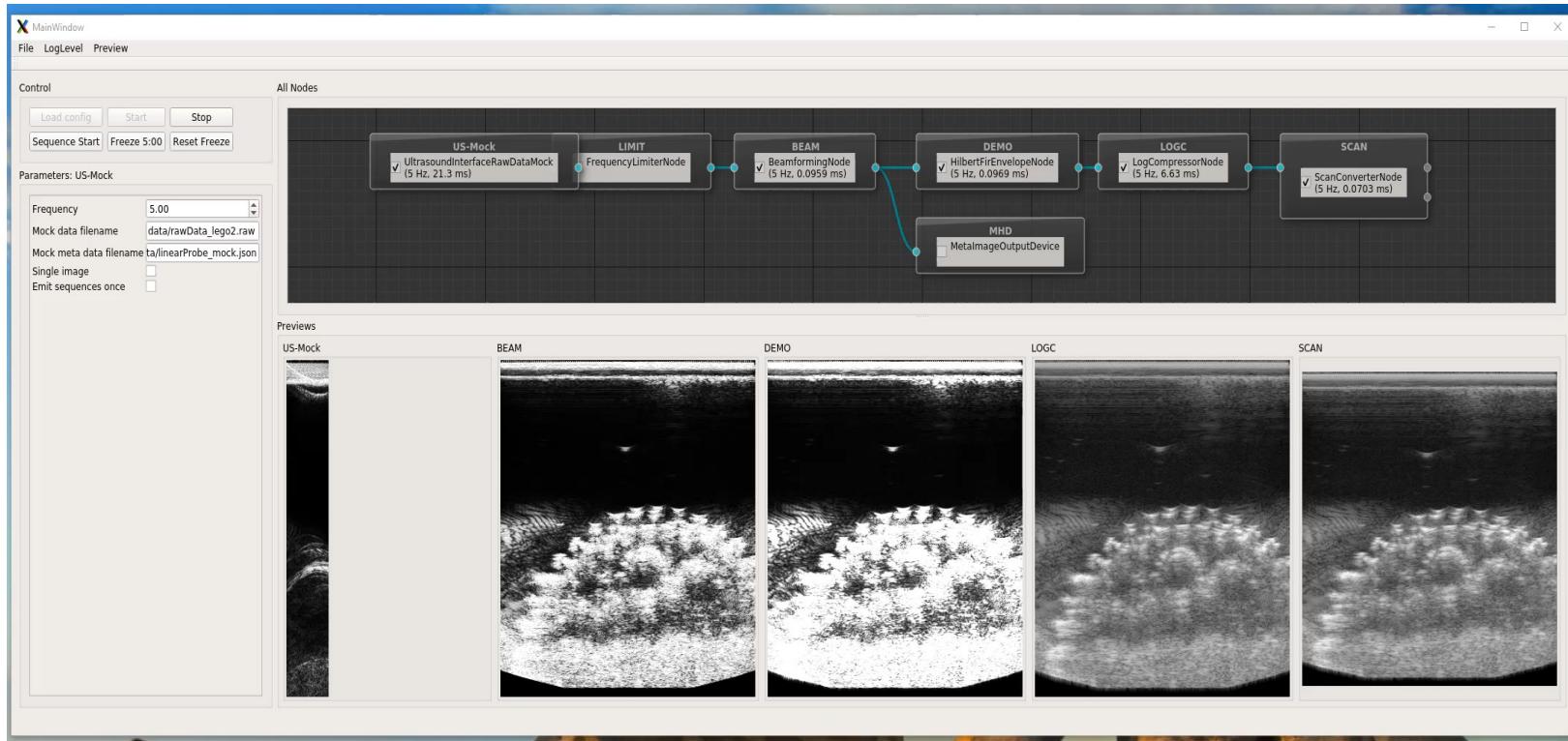
- oneAPI provides high level language(DPC++) to programming FPGA, which is more flexible, easy to learn, easy to develop, easy to debug.
- To use oneAPI programing for FPGA, Professional knowledge of FPGA is required.

```
424 template <typename InputType, typename OutputType>
425 void buf_fpga_scanConvert2D(
426     uint32_t numScanlines,
427     uint32_t numSamples,
428     uint32_t width,
429     uint32_t height,
430     InputType* scanlines,
431     OutputType* image,
432     sycl::accessor<fpga_data_load, 1, sycl::access::mode::read> fpga_data_load_acc)
433 {
434     uint32_t sIdx;
435     float wX;
436     float wY;
437     float val;
438     int32_t temp;
439     uint32_t buffer_index;
440     uint32_t buffer_1;
441     uint32_t buffer_2;
442     uint32_t buffer_3;
443     int Index_e = 0;
444
445     // FPGA specific attributes
446     [[intelfpga::max_replicates(4, intelfpga::doublepump]] float buf1[BUFFER_SIZE];
447     [[intelfpga::max_replicates(4, intelfpga::doublepump]] float buf2[BUFFER_SIZE];
448     [[intelfpga::max_replicates(4, intelfpga::doublepump]] float buf3[BUFFER_SIZE];
449
450     int buf_index = -1;
451     int Index = 0;
452
453     // preload buffer from global memory.
454     for (uint32_t i = 0; i < BUFFER_SIZE; i++)
455     {
456         buf1[i] = scanlines[i];
457         buf2[i] = scanlines[i + numScanlines];
458     }
```



Results and Performance

SUPRA GUI and DevCloud usage



Intel DevCloud usage – FPGA

The screenshot shows the Intel DevCloud Jupyter Notebook interface. On the left, there is a file browser window titled 'intelfpga-in-one /' showing files like build, data, emu_build, SupraLib, CMakeLists.txt, SUPRA-on-oneAPI-FPGA-all-in-one.ipynb (selected), and supralib.fpga. The main area is a Jupyter notebook titled 'SUPRA-on-oneAPI-FPGA-all-X'. It contains a welcome message: 'Welcome to Jupyter Notebooks on the Intel DevCloud for SUPRA-on-oneAPI-FPGA Project'. Below it, a note says 'This document contains the process of using Intel(R) oneAPI Base Toolkit build and run SUPRA on Intel FPGA.' A 'Table of Contents' section lists: 1. SUPRA introduction, 2. Build steps, 3. Performance. The '1. SUPRA introduction' section includes a note about the SUPRA project and a link to its GitHub page. The '2. Build steps' section has a sub-section '2.1 Download Ultrasound data and unzip files' with a code block:

```
[ ]: import wget
ultrasound_data_url = 'http://campar.in.tum.de/files/goeblr/mockData_linearProbe.zip'
config_file_url = 'https://github.com/IFL-CAMP/supra/raw/master/config/configDemo.xml'

!rm -rf data
!mkdir data
```

Intel DevCloud: <https://devcloud.intel.com/oneapi/>

SUPRA performance on Intel hardware

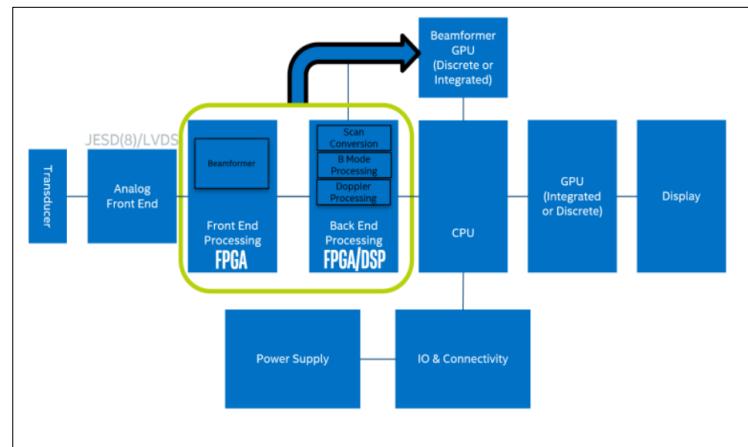
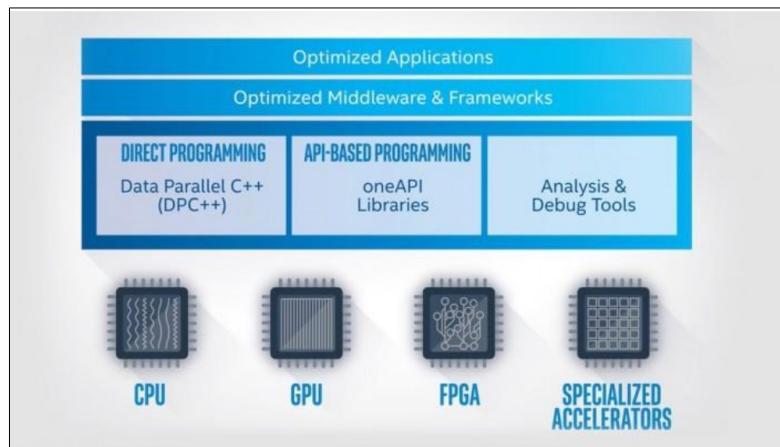
SUPRA Node	oneAPI (ms) – UHD630	Tiger lake Iris Xe	oneAPI - DG1(WA)	oneAPI – Arria 10
RxBeamforming	9.24	4.36	3.81	5.94
HilbertFirEnvelope	1.50	0.73	0.65	2.61
LogCompressor	0.27	0.1	0.08	0.34
ScanConverter	2.65	2.22	1.14	5.66
Total	13.66	7.41	5.68	5.94(max)

For the source code, please refer to: <https://github.com/intel/supra-on-oneapi>

For other vendors hardware performance, please refer to: <https://doi.org/10.1007/s11548-018-1750-6>

Summary

- Unified programming framework/language to implement medical algorithm accelerations on Intel HW
- Samples to implement Ultrasound beamforming on Intel xGPU
- Samples to implement Ultrasound beamforming on Intel FPGA
- Possibility to integrate algorithm acceleration and AI inference on a heterogenous compute system(Intel oneAPI and OpenVINO)
- Future Intel acceleration hardware (xPU) support



Thanks for your time!

The Intel logo is displayed in white against a solid blue background. The word "intel" is written in a lowercase sans-serif font. A small, solid cyan square is positioned above the top of the letter "i". The letter "i" has a vertical stroke extending upwards from its main body. The letter "t" has a vertical stroke extending downwards from its main body. The letter "e" has a vertical stroke extending upwards from its main body. The letter "l" has a vertical stroke extending upwards from its main body. A registered trademark symbol (®) is located at the bottom right of the "el" cluster.

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